T-Gate Aligned Nanotube Radio Frequency Transistors and Circuits with Superior Performance

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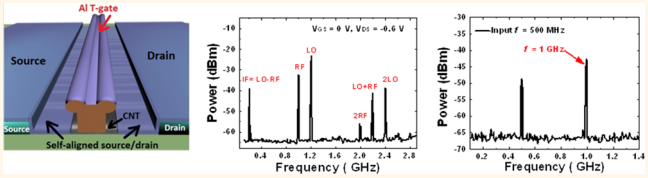
ABSTRACT In this paper, we applied self-aligned T-gate design to aligned carbon nanotube array transistors and achieved an extrinsic current-gain cutoff frequency (f_t) of 25 GHz, which is the best on-chip performance for nanotube radio frequency (RF) transistors reported to date. Meanwhile, an intrinsic current-gain cutoff frequency up to 102 GHz is obtained, comparable to the best value reported for nanotube RF transistors. Armed with the excellent extrinsic RF performance, we performed both single-tone and two-tone measurements for aligned nanotube transistors at a frequency up to 8 GHz. Furthermore, we utilized T-gate aligned nanotube transistors to construct mixing and frequency doubling analog circuits operated in gigahertz frequency regime. Our results confirm the great potential of nanotube-based circuit applications and indicate that nanotube transistors are promising building blocks in high-frequency electronics.



KEYWORDS: carbon nanotube arrays · chemical vapor deposition · self-aligned · radio frequency transistor · T-gate · linearity · mixer · frequency doubling · analog circuit

Carbon nanotubes have attracted extensive attention in advanced electronics over a decade due to unique characteristics of high mobility, large transconductance, small dimension, and low capacitance.[1−16] Among these applications, analog electronics are of great importance and only require high transconductance but not high on/off ratio for RF transistors.[9−16] Meanwhile, through significant research efforts, excellent radio frequency (RF) performance has been demonstrated in previous publications using nanotube networks/arrays from preseparated high-purity semiconducting nanotube solution and as-grown parallel nanotube arrays synthesized by chemical vapor deposition (CVD).[11,12,15,16] Kocabas *et al.* made radio frequency transistors based on CVD synthesized aligned nanotube arrays and reported an extrinsic current-gain cutoff frequency of 5 GHz.[17] Nougaret *et al.* also achieved an on-chip performance of 15 GHz current-gain cutoff frequency by using dielectrophoresis to assemble separated high-purity semiconducting nanotubes.[13] Recently, an extrinsic current-gain cutoff frequency of 7 GHz has been reported for dielectrophoresis-assembled separated high-purity semiconducting nanotube array transistors with channel lengths scaled down to 100 nm.[16] Those transistors based on separated semiconducting nanotubes showed intrinsic current-gain cutoff frequencies around 80[13] and 153 GHz[16] after de-embedding. It was also discussed that good alignment of nanotubes is important for RF transistor performance.[16] The above-mentioned work has shown the great potential of nanotube-based transistors for future high-frequency applications. However, the integration of large-area aligned nanotube arrays based on preseparated semiconducting nanotube solution through the dielectrophoresis (DEP) method still remains an obstacle for scalable fabrication of nanotube-based electronics.[12,16] Therefore, to advance the development of nanotube analog circuits, scalable assembling of nanotubes and fabrication of high performance transistors is required.

We note that there are two ways to assemble large-scale nanotube material. One is the wafer-scale dispersion of high-purity preseparated semiconducting nanotube solution using the method of surface functionalization.[15,18,19] This dispersion method is a scalable room-temperature processing procedure and the high-purity of

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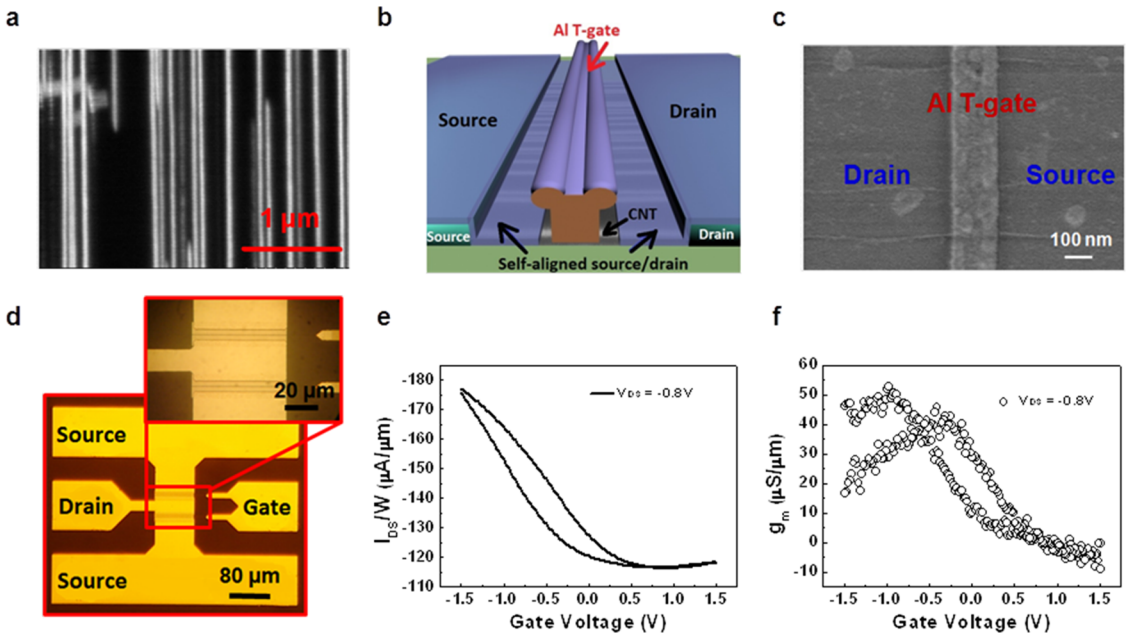

Figure 1. (a) SEM image of aligned carbon nanotubes on a quartz substrate (density: 5 SWNTs/μm). (b) Schematic of a self-aligned T-gate aligned nanotube RF transistor. (c) Top-view SEM image of a T-shape gate transistor (T-gate cap, 150 nm; base, ~100 nm). (d) Optical image of a T-gate aligned nanotube RF transistor with a channel width of 80 μm. Inset is a zoom-in image of the active transistor region. (e) Transfer characteristics of T-gate aligned nanotube RF transistor. (f) Scaled transconductance (g_m/W) *vs* gate voltage (V_{gs}) curve for aligned nanotube RF transistor.

semiconducting nanotubes brings benefits to transistor performance. We have reported decent RF performance with nanotube networks prepared using this method.[15] However, this assembly method provides nanotube networks instead of aligned nanotube arrays. Another solution to achieve scalable assembling of nanotubes is chemical vapor deposition.[20−24] In this method, large-area horizontally aligned single-wall carbon nanotubes (SWCNTs) can be obtained on certain crystalline substrates like quartz or sapphire. In this way, this kind of parallel nanotube provides a great platform for wafer-scale fabrication of RF transistors and circuits. In addition, aligned geometry of as-grown nanotubes allows the gate to control each nanotube without any screening. In contrast, nanotube networks prepared using solution-processed separated nanotubes usually have nanotubes stacked on top of each other (Figure S1), and the gate electric field for some nanotubes can be screened by other nanotubes nearby or on top, therefore, leading to weakened gate control. Furthermore, while aligned nanotubes provide direct conduction paths between source and drain, nanotube networks may have tube-to-tube junctions in the channel, which may lead to reduced conductance. It is therefore very important to further explore the potential of aligned CVD nanotubes for RF transistors and circuits.

Our group has recently developed a self-aligned T-shape gate fabrication approach for high-performance RF transistors and has successfully applied it to both graphene and solution-processed separated high-purity nanotube networks.[15,25] With this design, the parasitic effects including fringe gate capacitance, access resistance, and gate charging resistance can be significantly reduced. Furthermore, the channel length was scaled down to 140 nm and gate dielectric was reduced to 2−3 nm Al_2O_3, which led to the quasi-ballistic and quasi-quantum capacitance operation for nanotubes.[15] In this work, we have further applied the self-aligned T-gate RF transistor design to CVD-synthesized aligned nanotube arrays, so that we can combine the advantages of having aligned nanotubes and the reduced parasitic provided by the self-aligned T-gate approach. An extrinsic current-gain cutoff frequency up to 25 GHz before any de-embedding procedure is achieved for T-gate aligned nanotube transistors, which is the highest extrinsic cutoff frequency reported to date for nanotube transistors. After de-embedding, the intrinsic cutoff frequency further goes up to 100 GHz regime, which is among the best value reported for nanotube-based radio frequency transistors. Armed with the excellent on-chip performance, we further analyzed the linearity properties and carried out am extensive analog circuit study including mixing and frequency doubling circuits. In this work, we demonstrated the self-aligned nanotube transistor-based analog circuits operated in gigahertz regime for the first time to the best of our knowledge. Our results reveal that nanotubes are very promising building blocks in the future high-frequency field.

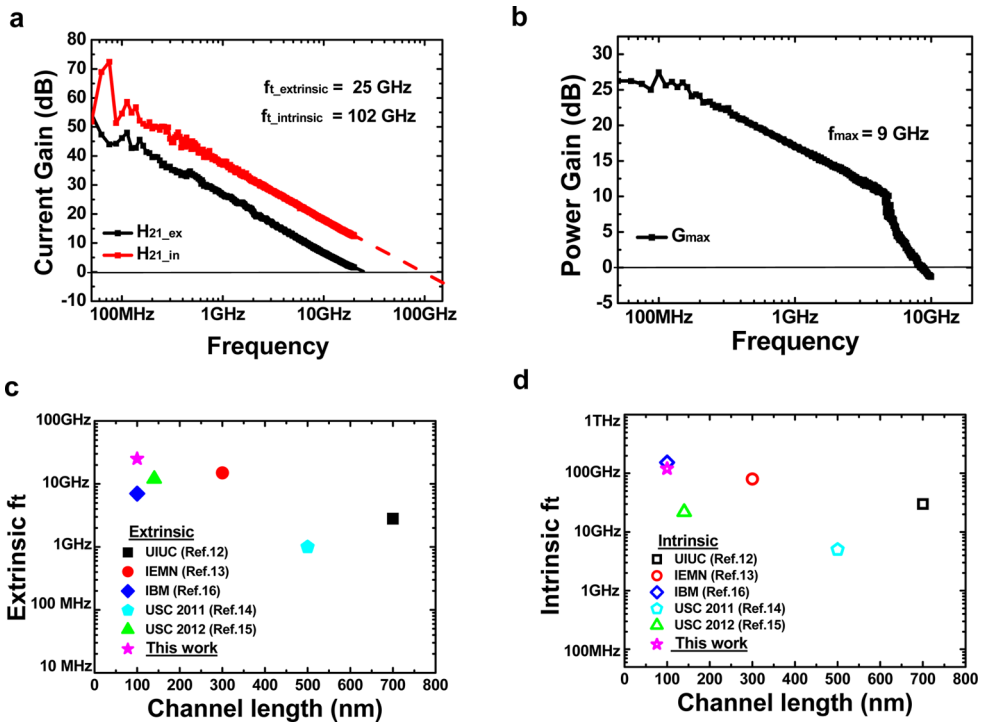

Figure 2. RF performance of a self-aligned T-gate aligned nanotube transistor. (a) Current gain (H_{21}) before (black curve) and after (red curve) the de-embedding procedure. (b) Extrinsic power gain (MAG) curve. (c,d) Extrinsic (c) and intrinsic (d) cutoff frequency *vs* channel length from previous publications and our work.

RESULTS AND DISCUSSION

Figure 1a shows a field emission scanned electron microscope (FESEM) image of aligned nanotube arrays on a quartz substrate with a density of 5 SWNTs/μm grown by CVD method. This CVD approach can produce aligned SWCNTs over complete wafers for wafer-scale fabrication, as we reported previously.[22] As we discussed in a previous report, self-aligned T-gate technology has been proven to be a good platform for carbon nanotube radio frequency device applications.[15] Details of the fabrication process can be found in the Methods section. Figure 1b exhibits the device schematic of a T-shaped gate aligned nanotube device. In Figure 1c, a top-view of the gate structure is presented with a cap size of 150 nm. The channel length of the gate structure in Figure 1c is estimated to be around 100 nm according to the inspection of cross-section from well-established recipe. The "ungated" region is estimated to be around 5−10 nm at each side of the gate structure. The length of the self-aligned Pd film region is about 4 μm extended from the first layer of source and drain patterned by photolithography. Due to the self-oxidization of the aluminum film of gate electrode, a thin layer of the Al_2O_3 dielectric (~3 nm) forms at the interface between the nanotube arrays and the gate metal. Based on our previous work, there is no leakage current observed at a bias as high as 3 V.[25] The gate capacitance of this T-gate structure is estimated to be around 1×10^{-9} F/m.[15] An optical image of the aligned nanotube RF transistor with an 80 μm channel width fabricated on quartz substrate is shown in Figure 1d.

Electrical measurements were carried out with the devices exposed to ambient air. The DC performance of the aligned nanotube RF transistor is characterized in Figure 1e,f. Figure 1e illustrates the transfer characteristics ($I_{DS}-V_{GS}$ curve) of an aligned nanotube T-gate device with a channel width of 80 μm and channel length of 100 nm. The top-gate characteristics were measured with V_{GS} swept from −1.5 to 1.5 V at drain bias V_{DS} of −0.8 V. More information can be found in the Supporting Information (Figure S2). The on/off ratio of this device is around 2 due to the coexistence of metallic and semiconducting nanotubes.[24,26] In spite of the relative low on/off ratio, the aligned nanotube transistor here shows high conductance (180 μA/μm), which is about six times higher than that of a transistor based on separated nanotube networks (30 μA/μm) with similar geometry and nanotube density.[15] Possible reasons for this difference in conductance may include different nanotube quality, as CVD-synthesized nanotubes are known to have high quality and nearly defect-free structures, and the possible presence of residual surfactants for solution-processed separated nanotubes. In addition, alignment of nanotube arrays can also help to improve conductance because of the lack of nanotube-to-nanotube junctions. Figure 1f presents the transconductance *versus* gate bias voltage (g_m-V_{GS}) curve with a peak transconductance up to 60 μS/μm. According to the information shown in

Figure 1f, the peak transconductance of this aligned nanotube transistor is about two times higher than that of the separated nanotube transistor published previously with a similar device structure and geometry.[15] As a result, aligned nanotube transistors with good DC performance in terms of high conductivity and transconductance enable us to further explore high-frequency applications. We note that this particular device shows relative small hysteresis, as shown in Figure 1e,f. This hysteresis may lead some variation in the RF measurement, such as variation in the gate voltage corresponding to the highest transconductance.

We further characterized the high-frequency performance of T-gate aligned carbon nanotube transistors in Figure 2. We measured the S-parameters of the transistor discussed in Figure 1 by using a vector network analyzer (VNA) with frequency ranging from 0.05 to 20 GHz. The probe tips were calibrated by using the off-wafer short-open-load-through (SOLT) standard procedure. The high-frequency performance of this device was derived from the as-measured S-parameters at $V_{TG} = -0.7$ V and $V_{DS} = -0.8$ V, where the optimal transconductance occurs. Figure 2a presents the current-gain (H_{21}) of the aligned nanotube RF transistor before and after de-embedding procedure. As shown in Figure 2a, the current−gain curves indicate an extrinsic cutoff frequency of 25 GHz and intrinsic cutoff frequency of 102 GHz. The extrinsic frequency performance of this aligned nanotube transistor in this work is one of the best reported to date for nanotube-based transistors. Figure 2b illustrates the power-gain curve of the aligned nanotube transistor and it shows an extrinsic unity power-gain frequency f_{max} of about 9 GHz. For comparison, recently published extrinsic and intrinsic radio frequency performances of nanotube-based RF transistors are shown in Figure 2c and d, respectively. Based on the data shown in Figure 2c, our work presents the highest extrinsic current-gain cutoff frequency (25 GHz). Furthermore, the intrinsic nanotube RF performance achieved in this work (102 GHz) is among the best performance for nanotube transistors, as illustrated in Figure 2d. Compared with previous reports,[15] the improvement of the cutoff frequency in our work results from the scaling of the channel length, excellent alignment, and good quality of nanotube arrays. We have made about 20 transistors with gate length around 100 to 140 nm, and they all show consistent values of f_t and f_{max}. These provide us the foundation to realize radio frequency circuits operated in gigahertz regime.

We analyzed the linearity performance of aligned nanotube transistors using a single-tone (1 dB compression point) and two-tone test (third-order intercept point). The schematic of the measurement set up is illustrated in Figure 3a. The device used in the

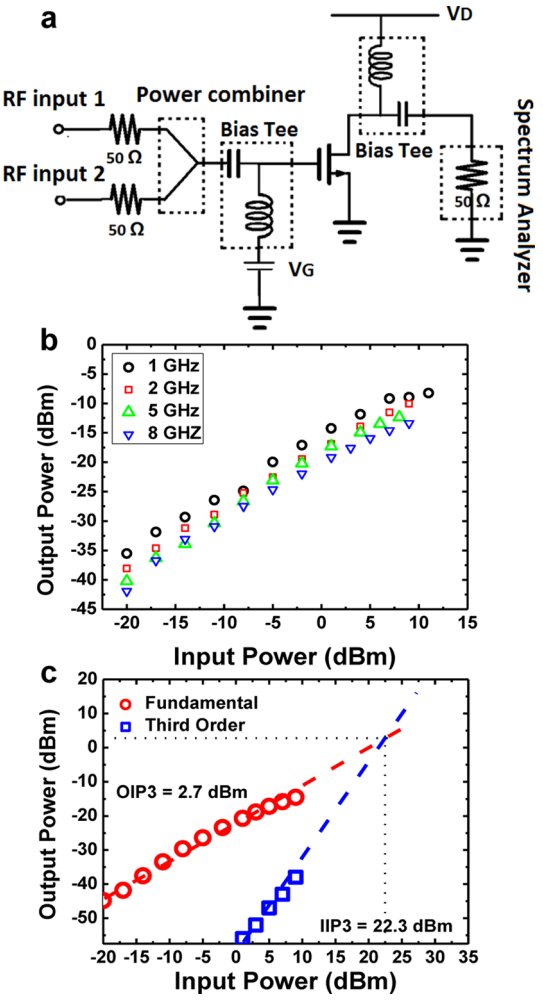

Figure 3. Linearity performance of a self-aligned T-gate aligned nanotube transistor. (a) Schematic of single/two tone test for an aligned nanotube transistor. (b) Output power of the fundamental *vs* input power. (c) Output power of the fundamental and third-order intermodulation as a function of the input power measured in the frequency region of 5 GHz.

circuit configuration has a unity power-gain frequency of 9 GHz. We first applied a single-tone signal with frequency range from 1 to 8 GHz to the gate of the aligned nanotube transistor and measured the output signal power level with a spectrum analyzer. Figure 3b shows the plots of extracted output power of fundamental as a function of input power at various frequencies. Based on the curves shown in Figure 3b, we obtain the 1 dB compression point for this nanotube device to be around 10 dBm for different frequencies. Details can be found in the Supporting Information (Figure S3). These P1dB values indicate that this nanotube transistor can operate linearly with an input power up to 10 dBm, which is consistent with the discussion about the linearity performance of carbon nanotube transistors reported recently.[14,15] Furthermore, it can be noticed that the power gain does not degrade much even when frequency goes up to relatively high

frequencies (8 GHz). In the two-tone measurement, we applied two-tone signals with adjacent frequencies to the gate of the aligned nanotube transistor through a power combiner as shown in Figure 3a. We conducted the two-tone test at 5 and 5.3 GHz. In Figure 3c, the power level of the fundamentals and third-order intermodulation ($2f_2-f_1$ or $2f_1-f_2$) are extracted as a function of input power. As shown in Figure 3c, the power of fundamentals and third-order intermodulation follow the slope of 10 and 30 dB/decade, consistent with theoretical rate. We obtained IIP3 of 22.3 dBm and OIP3 of 2.7 dBm at the third-order intercept point for the two-tone test at 5 and 5.3 GHz. IIP3 and OIP3 are important figures of merit capturing the linearity of the mixer. Our results compare favorably with previous publications.[14] For example, here we achieved the P1dB of 10 dBm at a frequency of 8 GHz, while previous work only studied the frequency range from 10 to 500 MHz.[14,15]

Armed with the above-mentioned linearity, we further applied aligned nanotube radio frequency transistors for analog circuits. The first example is the mixer. The aligned nanotube transistor-based mixer is configured by mixing the LO (local oscillation) and RF (radio frequency) signals at the gate (Figure 3a). Figure 4a shows the output spectrum of the mixer with the transistor biased at $V_{GS} = 0$ V and $V_{DS} = -0.6$ V. The RF input frequency f_{RF} is 1 GHz of power −14 dBm and the local oscillator frequency f_{LO} is 1.2 GHz of power −3.5 dBm. One can find the intermediate frequency (IF) f_{IF} at $f_{LO} - f_{RF} = 200$ MHz and $f_{LO} + f_{RF} = 2.2$ GHz. The conversion gain of this nanotube-transistor-based mixer is about −24.5 dB with the IF output power of −38.5 dBm as shown in Figure 4a. Figure 4b shows that the conversion gain varied as the gate voltage swept from −1 to 1 V. The first peak of the conversion gain at $V_{GS} = -0.7$ V may result from the maximum transconductance g_m at this bias (Figure 1f). While the second peak occurs nearby the minimum current point of the $I_{DS}-V_{GS}$ curve (Figure 1e), and it has been discussed that the minimum current point is the optimal bias point for the conversion gain of an ambipolar transistor-based mixer previously.[27] We further achieved mixing for the frequency range from 1 to 8 GHz (Supporting Information, Figure S4). Figure 4c presents the conversion gain of the aligned nanotube RF transistor as a function of applied frequency. The result illustrates that conversion gain does not decrease much even when the frequency goes up to 8 GHz. On the basis of the information above, carbon nanotube transistors show great potential for mixer applications.

Other than amplifiers and mixers, aligned carbon nanotube transistors can find applications in frequency doubling circuits based on the ambipolar transport property.[28] Figure 5a shows the transfer characteristics

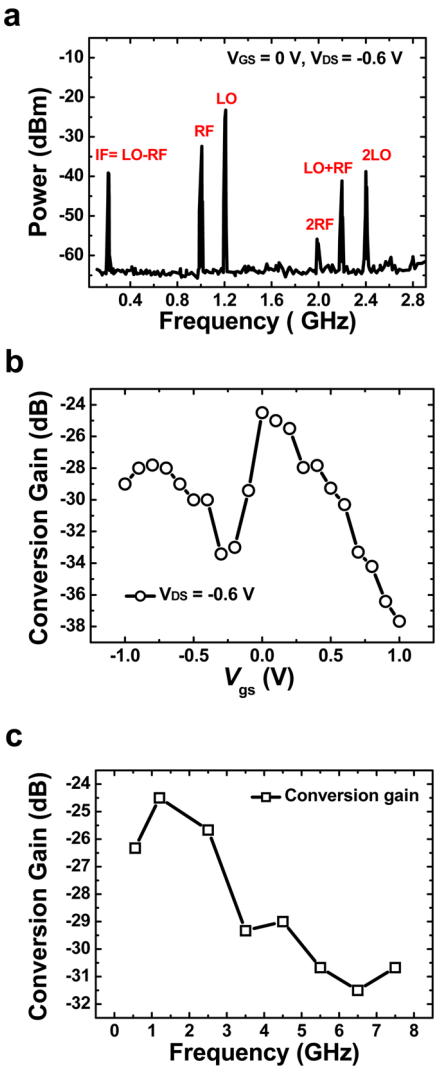

Figure 4. Mixer application of self-aligned T-gate aligned nanotube transistor. (a) Output spectrum for an aligned nanotube mixer, which shows the first, second, and third order mixing products with a high conversion gain of −24.5 dB at LO power of −3.5 dBm. (b) Conversion gain *vs* gate voltage for an aligned nanotube mixer. (c) Conversion gain *vs* frequency for an aligned nanotube mixer.

of an aligned carbon nanotube array transistor. We can see that this nanotube transistor shows ambipolar transport around the minimum current point (V_{MCP} = 1.2 V). A frequency doubler based on nanotube RF device can be achieved with a circuit diagram as shown in Figure 5b. For transistors with ambipolar transport, the transfer characteristic ($I_{DS}-V_{GS}$) resembles a parabolic curve near the minimal current point, and therefore has a squared term in the Taylor series expansion approximation. When the input gate voltage signal in Figure 5b is a sinusoidal wave biased around the minimal current point with frequency ω ($V_{GS} = V_{MCP} + A \sin \omega t$), the output signal would contain a term of $(\sin \omega t)^2$, which leads to an output at the double frequency (2ω). A current source with I_{dd} = 830 μA is connected to the drain electrode of the carbon

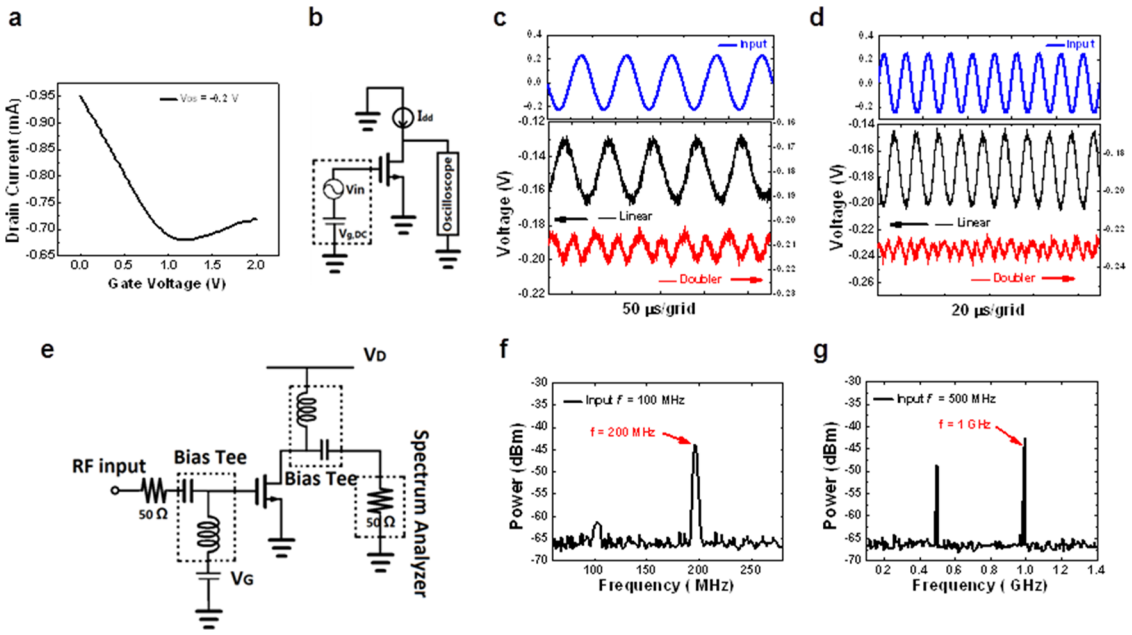

Figure 5. Frequency doubler application of self-aligned T-gate aligned nanotube transistor. (a) $I_{DS}-V_{GS}$ curve of an ambipolar aligned nanotube transistor. (b) Circuit schematic of an aligned nanotube frequency doubler with measurement setup using an oscilloscope. (c, d) Input and output waveforms of frequency doubler in linear amplification region and doubler region with sinusoidal wave with input V_{pp} = 450 mV at frequency of 10 kHz (c) and input V_{pp} = 500 mV at a frequency of 50 kHz (f). (e) Schematic of a frequency doubler with measurement setup using a spectrum analyzer. (f, g) Output spectrum of a frequency doubler with a 100 MHz input signal with power level of 0 dBm (f) and a 500 MHz input signal with power level of 5 dBm (g).

nanotube transistor. In Figure 5c, we added a 10 kHz input signal with a peak-to-peak a.c. voltage V_{pp} = 450 mV to a DC voltage $V_{g,DC}$ = 0.2 V (black curve) and $V_{g,DC}$ = 1.2 V (red curve) to the gate of the nanotube transistor, separately. The output waveforms from different bias regions are illustrated in Figure 5c. Based on Figure 5c, the red curve biased around the minimum current point presents a sinusoidal wave with a doubled frequency. In comparison, the black curve biased in the linear amplification region shows a sinusoidal wave with the same frequency as the input signal. In Figure 5d, we also achieved the doubled frequency output (red curve) with 50 kHz input signal of V_{pp} = 500 mV biased at $V_{g,DC}$ = 1.5 V. Then we further characterized the frequency doubling function of the aligned nanotube transistor up to the gigahertz regime with the help of a spectrum analyzer, as shown in the schematic diagram of Figure 5e. The output spectra captured by the spectrum analyzer are presented in Figure 5f,g. In Figure 5f, it can be noticed that the output spectrum peak is at 200 MHz, corresponding to an input signal with 100 MHz frequency, which shows excellent frequency doubling function. As shown in Figure 5g, even when the input frequency increases up to 500 MHz, the output spectrum still has a strong concentration at 1 GHz frequency. We also performed the doubler measurement with an input frequency of 1 GHz, and the results show that the output power concentrated mainly at the doubled frequency of 2 GHz (Supporting Information, Figure S5). Our results clearly show that aligned carbon nanotube transistors with the ambipolar transport property can serve as a frequency doubler up to gigahertz regime in high-frequency applications. Our frequency doubler performance measured up to 1 GHz compares favorably with previously reported results for carbon nanotubes. For instance, Wang *et al.* reported a frequency doubler based on nanotube transistor operated in the 1 kHz region.[28] We attribute the good performance of our transistors to the self-aligned T-gate transistor design and the resulting high extrinsic f_t and f_{max}.

CONCLUSION

In summary, we constructed T-gate aligned nanotube array RF transistors with the extrinsic current-gain cutoff frequency of 25 GHz as the best on-chip performance for nanotube RF transistors reported to date. Correspondingly, the intrinsic current-gain cutoff frequency of 102 GHz was achieved after de-embedding, which is among the highest value for nanotube-based RF transistors. Furthermore, we studied the linearity properties of aligned nanotube transistors through single-tone (P1dB) and two-tone (IP3) measurements with direct 50 Ω termination up to 8 GHz. Armed with the excellent extrinsic RF performance, we configured nanotube-based circuits including a mixer and a frequency doubler, operated in the gigahertz frequency regime. Our work confirms the great potential of

carbon nanotubes for radio frequency applications, and the self-aligned T-gate RF transistor design may become a building block for future nanotube-based RF transistors and circuits.

METHODS

Large-scale aligned nanotube arrays were synthesized on quartz substrates by using ethanol as carbon feedstock for CVD nanotube synthesis. The quartz substrate with deposited Fe catalyst film was loaded into the CVD furnace. During the synthesis, 120 standard cubic centimeter (sccm) of hydrogen (H_2) was used during the ramping up step, and then 60 sccm of Ar flow was added into the system through an ethanol bubbler (kept at 0 °C) for growth conducted at 900 °C. An average density of 5 tubes/μm was achieved using this CVD process. Then ground−signal−ground (GSG) coplanar waveguide structures were patterned directly on the quartz substrate for source and drain electrodes (5/50 nm of Ti/Au) of nanotube RF transistors by photolithography, followed by O_2 plasma etching of nanotubes outside the active channel region. Then the sample was annealed in H_2 atmosphere at 300 °C for half an hour. By using bilayer electron beam resists of different sensitivities (copolymer of methyl methacrylate and methacrylic acid P(MMA-MAA) as top layer, and polymethyl methacrylate (PMMA) with 950k molecular weight as bottom layer), a T-shaped sidewall profile of the bilayer resist was achieved by exposing the center of the T-gate with high dosage and the left/right sides of the T-gate with lower dosage. Then the T-shaped gate (T-gate) stack was produced by a standard lift-off process after the deposition of 150 nm aluminum film. By heating the sample to 150 °C in air for about 1 h, the oxidation of aluminum T-gate in air formed a thin dielectric layer (~3 nm) at the interface between the nanotube array and the gate electrode. Finally, 10 nm palladium was deposited to form self-aligned source and drain with the T-gate as a shadow mask. No annealing was performed on the devices after deposition of the self-aligned Pd source and drain electrodes.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: AFM image of separated nanotube networks and CVD-synthesized aligned nanotubes (S1); DC performance of aligned nanotube transistors (S2); Single-tone measurement (S3); Mixer measurement (S4); Frequency doubling circuit measurement (S5); and De-embedding procedure (S6). This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Durkop, T.; Getty, S. A.; Cobas, E.; Fuhrer, M. S. Extraordinary Mobility in Semiconducting Carbon Nanotubes. *Nano Lett.* **2004**, *4*, 35–39.
2. Zhou, X. J.; Park, J. Y.; Huang, S. M.; Liu, J.; McEuen, P. L. Band Structure, Phonon Scattering, and the Performance Limit of Single-Walled Carbon Nanotube Transistors. *Phys. Rev. Lett.* **2005**, 95.
3. Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. Logic Circuits with Carbon Nanotube Transistors. *Science* **2001**, *294*, 1317–1320.
4. Derycke, V.; Martel, R.; Appenzeller, J.; Avouris, P. Carbon Nanotube Inter- and Intramolecular Logic Gates. *Nano Lett.* **2001**, *1*, 453–456.
5. Liu, X. L.; Lee, C.; Zhou, C. W.; Han, J. Carbon Nanotube Field-Effect Inverters. *Appl. Phys. Lett.* **2001**, *79*, 3329–3331.
6. Javey, A.; Wang, Q.; Ural, A.; Li, Y. M.; Dai, H. J. Carbon Nanotube Transistor Arrays for Multistage Complementary Logic and Ring Oscillators. *Nano Lett.* **2002**, *2*, 929–932.
7. Chen, Z. H.; Appenzeller, J.; Lin, Y. M.; Sippel-Oakley, J.; Rinzler, A. G.; Tang, J. Y.; Wind, S. J.; Solomon, P. M.; Avouris, P. An Integrated Logic Circuit Assembled on a Single Carbon Nanotube. *Science* **2006**, *311*, 1735–1735.
8. Ryu, K.; Badmaev, A.; Wang, C.; Lin, A.; Patil, N.; Gomez, L.; Kumar, A.; Mitra, S.; Wong, H. S. P.; Zhou, C. W. Cmos-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes. *Nano Lett.* **2009**, *9*, 189–197.
9. Li, S. D.; Yu, Z.; Yen, S. F.; Tang, W. C.; Burke, P. J. Carbon Nanotube Transistor Operation at 2.6 Ghz. *Nano Lett.* **2004**, *4*, 753–756.
10. Le Louarn, A.; Kapche, F.; Bethoux, J. M.; Happy, H.; Dambrine, G.; Derycke, V.; Chenevier, P.; Izard, N.; Goffman, M. F.; Bourgoin, J. P.; et al. Intrinsic Current Gain Cutoff Frequency of 30 Ghz with Carbon Nanotube Transistors. *Appl. Phys. Lett.* **2007**, 90.
11. Kocabas, C.; Kim, H. S.; Banks, T.; Rogers, J. A.; Pesetski, A. A.; Baumgardner, J. E.; Krishnaswamy, S. V.; Zhang, H. Radio Frequency Analog Electronics Based on Carbon Nanotube Transistors. *Proc. Natl. Acad. Sci. U.S.A.* **2008**, *105*, 1405–9.
12. Kocabas, C.; Dunham, S.; Cao, Q.; Cimino, K.; Ho, X. N.; Kim, H. S.; Dawson, D.; Payne, J.; Stuenkel, M.; Zhang, H.; et al. High-Frequency Performance of Submicrometer Transistors That Use Aligned Arrays of Single-Walled Carbon Nanotubes. *Nano Lett.* **2009**, *9*, 1937–1943.
13. Nougaret, L.; Happy, H.; Dambrine, G.; Derycke, V.; Bourgoin, J. P.; Green, A. A.; Hersam, M. C. 80 Ghz Field-Effect Transistors Produced Using High Purity Semiconducting Single-Walled Carbon Nanotubes. *Appl. Phys. Lett.* **2009**, *94*, 243505.
14. Wang, C.; Badmaev, A.; Jooyaie, A.; Bao, M. Q.; Wang, K. L.; Galatsis, K.; Zhou, C. W. Radio Frequency and Linearity Performance of Transistors Using High-Purity Semiconducting Carbon Nanotubes. *ACS Nano* **2011**, *5*, 4169–4176.
15. Che, Y. C.; Badmaev, A.; Jooyaie, A.; Wu, T.; Zhang, J. L.; Wang, C.; Galatsis, K.; Enaya, H. A.; Zhou, C. W. Self-Aligned T-Gate High-Purity Semiconducting Carbon Nanotube Rf Transistors Operated in Quasi-Ballistic Transport and Quantum Capacitance Regime. *ACS Nano* **2012**, *6*, 6936–6943.
16. Steiner, M.; Engel, M.; Lin, Y. M.; Wu, Y. Q.; Jenkins, K.; Farmer, D. B.; Humes, J. J.; Yoder, N. L.; Seo, J. W. T.; Green, A. A.; et al. High-Frequency Performance of Scaled Carbon Nanotube Array Field-Effect Transistors. *Appl. Phys. Lett.* **2012**, 101.
17. Kocabas, C.; Dunham, S.; Cao, Q.; Cimino, K.; Ho, X. N.; Kim, H. S.; Dawson, D.; Payne, J.; Stuenkel, M.; Zhang, H.; et al. High-Frequency Performance of Submicrometer Transistors That Use Aligned Arrays of Single-Walled Carbon Nanotubes. *Nano Lett.* **2009**, *9*, 1937–1943.
18. Wang, C.; Zhang, J. L.; Ryu, K. M.; Badmaev, A.; De Arco, L. G.; Zhou, C. W. Wafer-Scale Fabrication of Separated Carbon Nanotube Thin-Film Transistors for Display Applications. *Nano Lett.* **2009**, *9*, 4285–4291.
19. Wang, C.; Zhang, J. L.; Zhou, C. W. Macroelectronic Integrated Circuits Using High-Performance Separated Carbon Nanotube Thin-Film Transistors. *ACS Nano* **2010**, *4*, 7123–7132.
20. Han, S.; Liu, X. L.; Zhou, C. W. Template-Free Directional Growth of Single-Walled Carbon Nanotubes on a- and R-Plane Sapphire. *J. Am. Chem. Soc.* **2005**, *127*, 5294–5295.
21. Kocabas, C.; Hur, S. H.; Gaur, A.; Meitl, M. A.; Shim, M.; Rogers, J. A. Guided Growth of Large-Scale, Horizontally

Aligned Arrays of Single-Walled Carbon Nanotubes and Their Use in Thin-Film Transistors. *Small* **2005**, *1*, 1110–1116.
22. Ryu, K.; Badmaev, A.; Wang, C.; Lin, A.; Patil, N.; Gomez, L.; Kumar, A.; Mitra, S.; Wong, H. S. P.; Zhou, C. W. Cmos-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes. *Nano Lett.* **2009**, *9*, 189–197.
23. Wang, C. A.; Ryu, K. M.; De Arco, L. G.; Badmaev, A.; Zhang, J. L.; Lin, X.; Che, Y. C.; Zhou, C. W. Synthesis and Device Applications of High-Density Aligned Carbon Nanotubes Using Low-Pressure Chemical Vapor Deposition and Stacked Multiple Transfer. *Nano Res.* **2010**, *3*, 831–842.
24. Che, Y. C.; Wang, C.; Liu, J.; Liu, B. L.; Lin, X.; Parker, J.; Beasley, C.; Wong, H. S. P.; Zhou, C. W. Selective Synthesis and Device Applications of Semiconducting Single-Walled Carbon Nanotubes Using Isopropyl Alcohol as Feedstock. *ACS Nano* **2012**, *6*, 7454–7462.
25. Badmaev, A.; Che, Y. C.; Li, Z.; Wang, C.; Zhou, C. W. Self-Aligned Fabrication of Graphene Rf Transistors with T-Shaped Gate. *ACS Nano* **2012**, *6*, 3371–3376.
26. Reich, S.; Li, L.; Robertson, J. Control the Chirality of Carbon Nanotubes by Epitaxial Growth. *Chem. Phys. Lett.* **2006**, *421*, 469–472.
27. Madan, H.; Hollander, M.; LaBella, M.; Cavalero, R.; Snyder, D.; Robertson, J.; Datta, S. Record High Conversion Gain Ambipolar Graphene Mixer at 10 Ghz Using Scaled Gate Oxide. 2012 IEEE International Electron Devices Meeting, December 10−12, San Francisco, CA, IEDM: Pikesville, MD, **2012**; pp 76−79.
28. Wang, Z. X.; Ding, L.; Pei, T. A.; Zhang, Z. Y.; Wang, S.; Yu, T.; Ye, X. F.; Peng, F.; Li, Y.; Peng, L. M. Large Signal Operation of Small Band-Gap Carbon Nanotube-Based Ambipolar Transistor: A High-Performance Frequency Doubler. *Nano Lett.* **2010**, *10*, 3648–3655.